ACORN 32K DYNAMIC RAM BOARD

UNIT DESCRIPTION

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1. INTRODUCTION

1.1 GENERAL

The 32K Dynamic RAM Board provides 32768 (32K) bytes of Dynamic Random Access Memory (DRAM) for a computer system. The Board is a 100 x 160mm Eurocard and is provided with a 64-way connector, for connection to the Acorn Bus.

The DRAM ICs are configured in two 16K by 8 bit Banks. Links on the Board provide individual address selection of four 8K sections of the DRAM, each section address begins at an even memory Block address. The Board can be partially equipped to provide 16K of DRAM. The Board is also provided with a paging facility.

The DRAM timing may be generated from a single clock input (e.g. 6502 §2) by an on-board Clock Circuit. Alternatively, three external synchronized clock inputs may be used. A Refresh Circuit refreshes the DRAM ICs between external Read or Write cycles, allowing access to the DRAM during any Central Processor Unit (CPU) cycle.

1.2 LEADING PARTICULARS

1.2.1 Mechanical

Construction : Single Eurocard PCB
Size : 100mm x 160mm

1.2.2 Power Supplies

+5V at 280mA.

1.2.3 Connections

Pin connections are given in Section 4.

Connector : Double-sided edge connector to Acorn Bus. TTL signal levels are used, 0V to +0.4V = logic '0', +2.4V = logic '1'.

2. CIRCUIT DESCRIPTION

A block diagram of the 32K Dynamic RAM Board is given on Figure 1. Reference should also be made to the circuit diagram, Figure 9. The DRAM Bank and Link location is given on Figure 2.

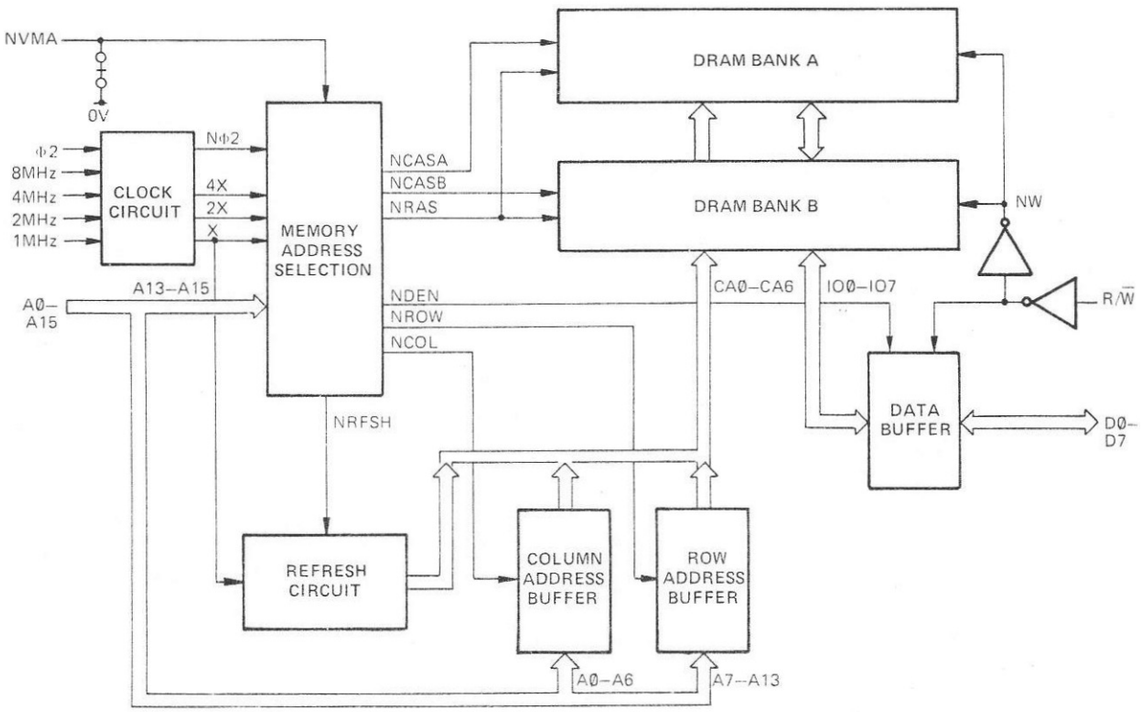


Figure 1. 32K Dynamic RAM Board Block Diagram

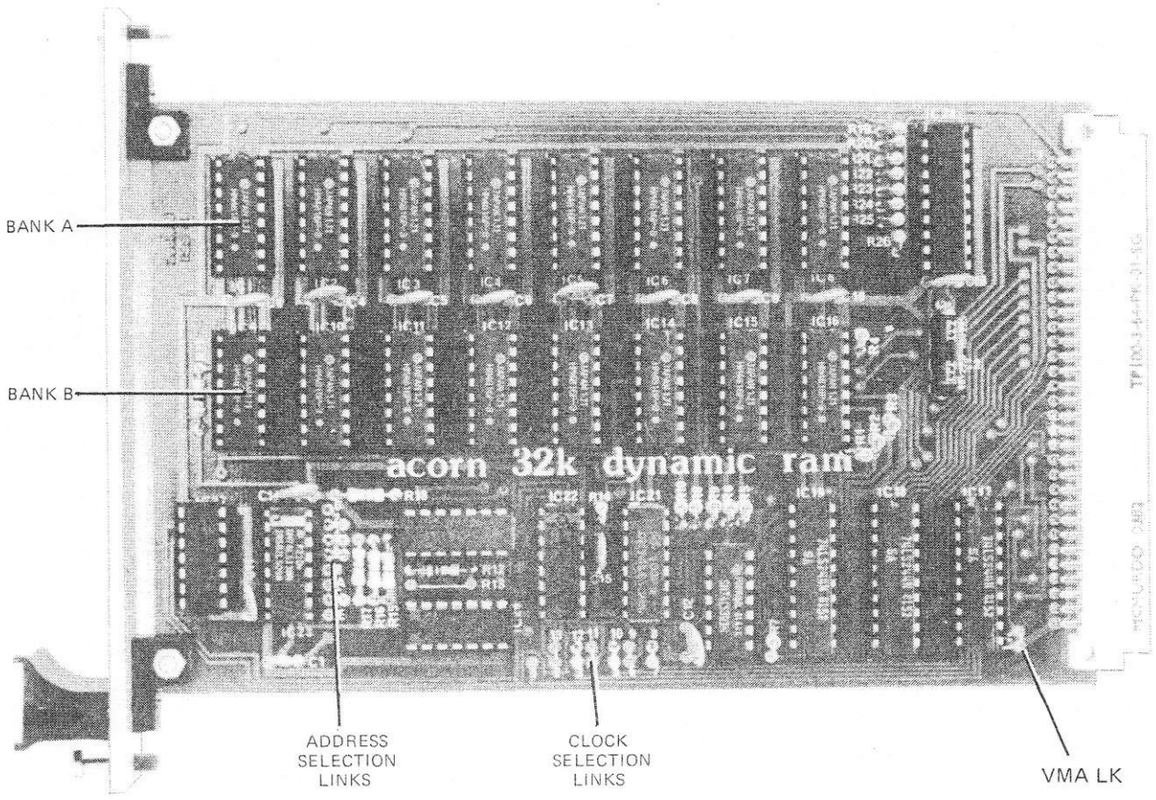


Figure 2. 32K DRAM Bank and Link Location

2.1 DYNAMIC RAM

The DRAM consists of two Banks of 4816 ICs, each IC having 16384 (16K) x 1 bit separately addressable memory locations. The 8 ICs in each Bank provide 16K 8 bit bytes of memory. The memory locations are addressed by seven address lines CA0--CA6, carrying multiplexed row and column addresses. The addresses are strobed into the ICs by the Row Address Strobe (NRAS) and Column Address Strobe (NCAS) signals. A Write (NW) enable signal determines whether a Write or Read operation is required. The DRAM ICs are refreshed by a row address on CA0–CA6 and a NRAS signal, the refresh address is cycled through the 128 row addresses by the Refresh Circuit, refer to para. 2. 4. The DRAM timing is given on Figure 3(a) 2MHz operation, and Figure 3(h) Local Oscillator operation.

2.2 MEMORY ADDRESS SELECTION

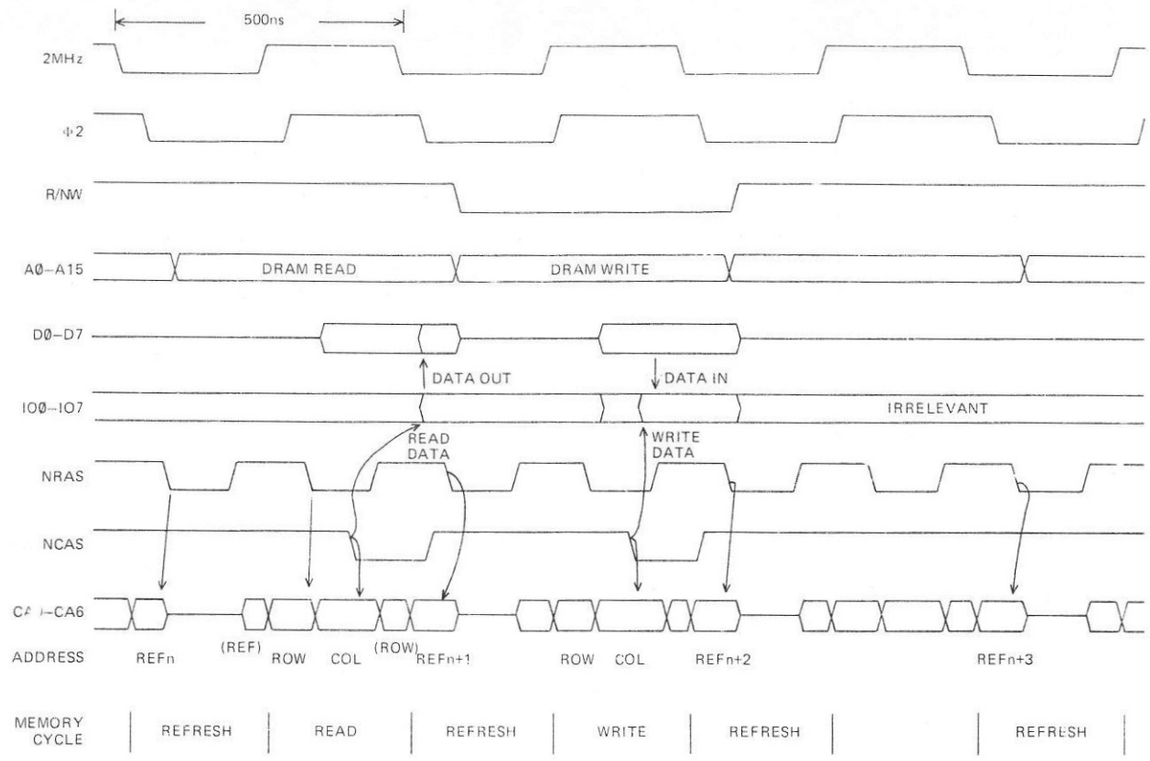
The Memory Address Selection Circuit decodes the address on the Acorn Bus lines A13—A15 to detect DRAM addresses, refer to Figure 4. The Row and Column Address Buffers are enabled in sequence by the Row Address Select (NROW) and Column Address Select (NCOL) signals, so that when a DRAM address is detected the appropriate NCASA or NCASB signal is generated. The two and column addresses are output from the Buffers onto the DRAM IC address lines A0—A6.

The Memory Address Selection Circuit also provides the NRAS and NCAS signals to strobe the addresses into the ICs. A Data Enable signal (LADEN) is set low to the Data Buffer to enable the transfer of data to or from the DRAM ICs.

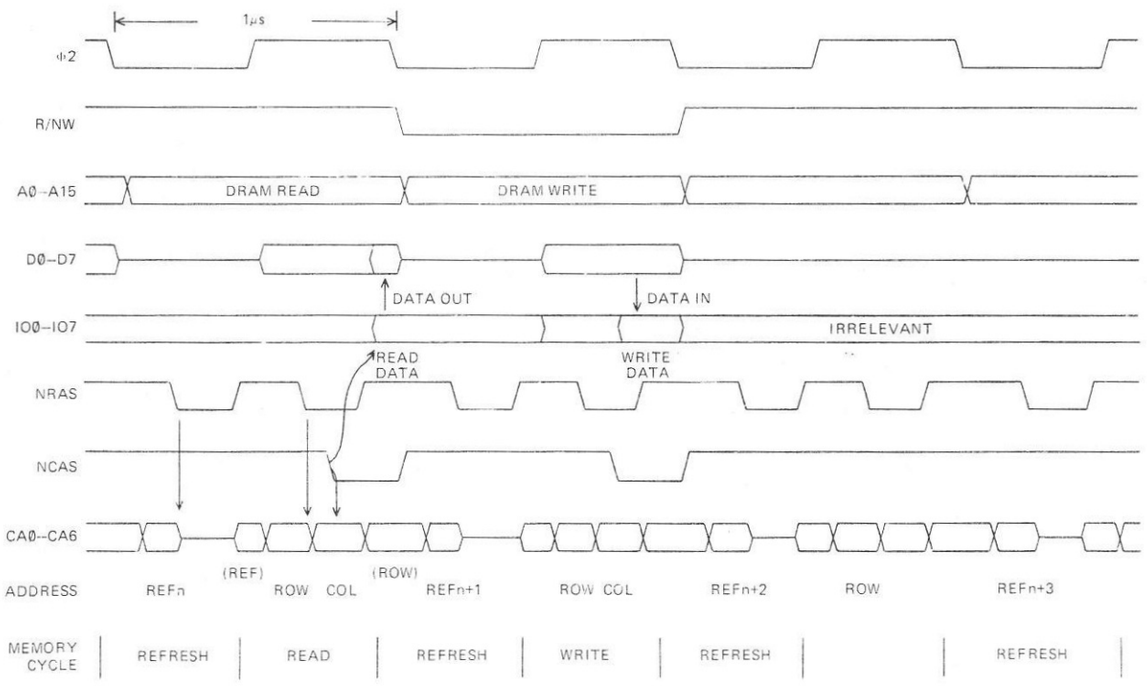
2.2.1 Address Decoding

The Acorn Bus address lines A15, A14 and A13 are decoded by IC23, during the CPU Phase 2 (§2) clock time. A low on the Valid Memory Address (NVMA) Acorn Bus signal enables IC23, when the Board is configured for memory paging, track. Link LK is cut. Otherwise, IC23 is enabled by the 0V connected to IC23/5 by Link LK. Enable G1, IC23/6 is connected to +5V. The inverted §2 signal at IC23/4 enables address decoding (provided NVMA is low), to provide a low on the selected output of IC23, refer to Table 1.

The DRAM addresses are determined by the configuration of the Address Selection Links. The normal



(a) 2MHz Operation



(b) Local Oscillator Operation

Figure 3. 32K DRAM Read, Write and Refresh Timing

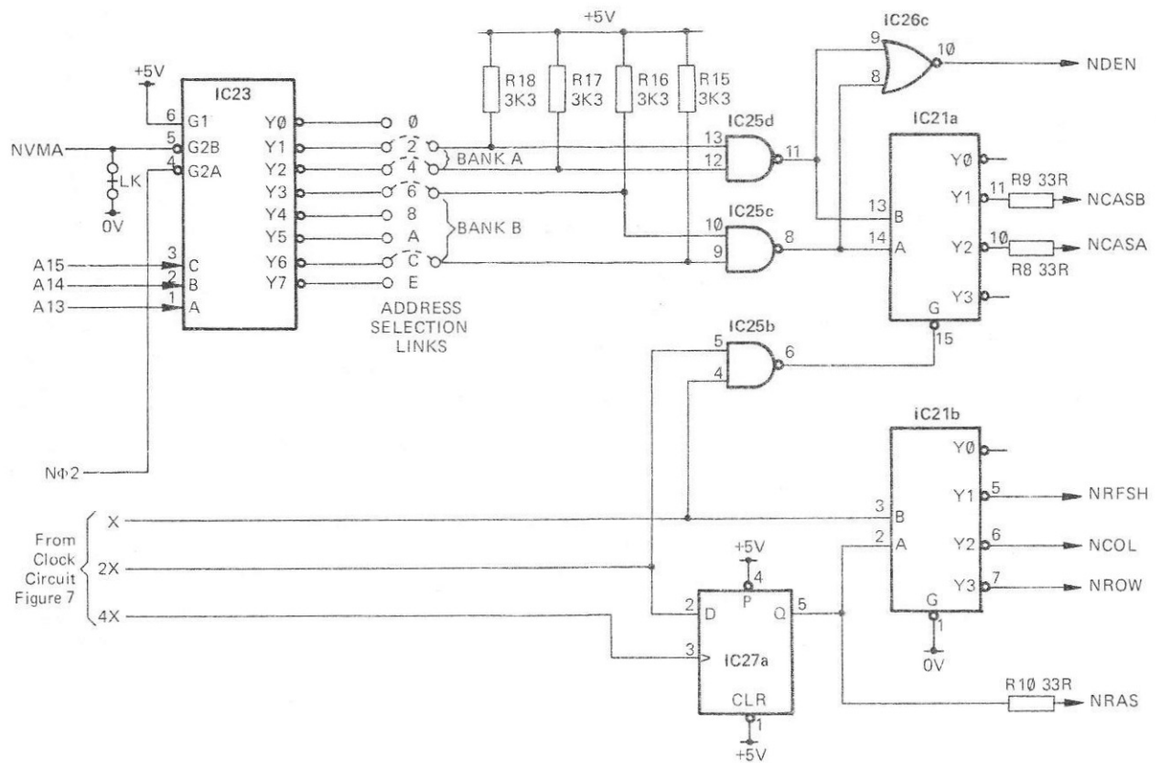


Figure 4. Memory Address Selection

§2	NVMA	A15	A14	A13	Selected Output '0'	Block Addressd (hex)	Link No.
0	X	X	X	X	None	None	
X	1	X	X	X	None	None	
1	0	1	1	1	Y7	E,F	E
1	0	1	1	0	Y6	C,D	C
1	0	1	0	1	Y5	A,B	A
1	0	1	0	0	Y4	8,9	B
1	0	0	1	1	Y3	6.7	6
1	0	0	1	0	Y2	4,5	4
1	0	0	0	1	Y1	2,3	2
1	0	0	0	0	Y0	0,1	0

Table 1. 32K DRAM Address Block Allocation

Acorn Computer configuration is given on the Memory Map Figure 5, alternatives can be configured by removing the links fitted and soldering new links to the required memory selection outputs, refer to Figure 5. Note that each link selects 8K (two Blocks) of memory addresses for one section of the DRAM.

Because the DRAM addresses are decoded to provide 4 starting points for RAM, and there are only 2 banks of IC's on the board, there is some redundancy in the address decoding. This means that the links associated with one bank must not be made so as to leave a gap of 1, 3 or 5 positions between them, If this restriction is not observed then one section of memory will respond to two address ranges, and data will be overwritten.

The 16K DRAM option can he equipped with 8 DRAM IC; in Bank B. The Address Selection Links are then required to give DRAM addresses 8000 (hex) to BFFF (hex), refer to Figure 5(c),

2.2.2 Address Signal Timing

When a DRAM address is decoded, NAND gates IC25c and IC25d (refer to Figure 4) give a high on the A or B input to IC21a. Any detected DRAM address gives a high on an input to NOR gate IC26c, to generate the NDEN signal low to the Data Buffer. NAND gate IC25b output low enables IC21a, to generates the appropriate NCASA or NCASB signal at the Column Address Strobe time (X and 2X high), refer to Figure 3.

The clock signals from the Clock Circuit, refer to para 2.3, generates the NRAS, NROW, NCOL and NRFSH signals as shown on Figure 6. The X and 2X clock signals also enable IC21a to generate NCAS signals as described above. The NROW, NCOL and NRFSH signals enable the outputs of the Row, Column and Refresh Address Buffers respectively, onto the DRAM address lines CA0—CA6, The row and refresh addresses are strobed by the NRAS signal negative edge, When a DRAM address is decoded, the column address is strobed by the appropriate NCASA or NCASB signal negative edge.

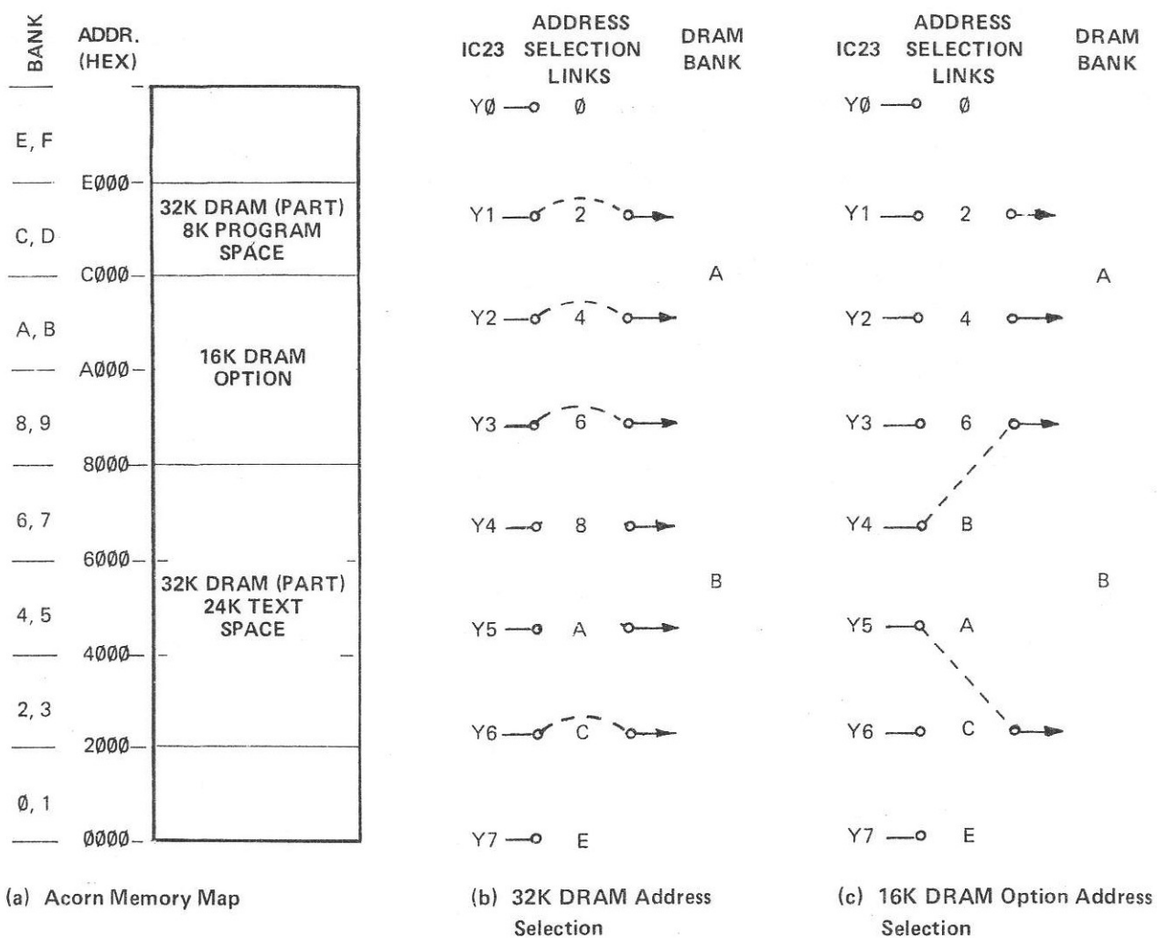


Figure 5. Acorn Memory Map and DRAM Address Selection

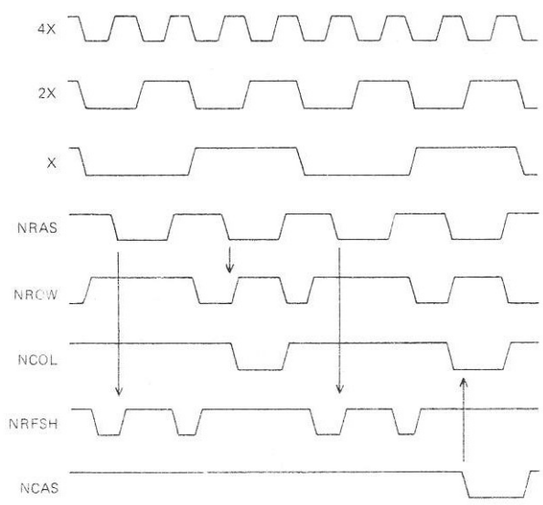


Figure 6. Address Signal Timing

2.3 CLOCK CIRCUIT

The Clock Circuit, refer to Figure 7, provides three synchronized signal outputs to the Memory Address Selection Circuit, either from the clock signals on the Acorn Bus (e.g. System 5) or from a local oscillator that is synchronized by the Phase 2 (§2) clock from a CPU (e.g. 6502 CPU).

Clock Selection Links are provided, refer to Figure 2, to select the appropriate clock signals as shown in Table 2. The clock signals are X, 2X and 4X, where X is the selected operating frequency: 1MHz or 2MHz.

2.3.1 Acorn Bus Clock Operation

The 32K DRAM Board is supplied to operate at 2MHz from the Acorn Bus clock signals, the appropriate links in the Clock Selection Links are soldered, in the positions indicated in Table 2, to connect the 8MHz, 4MHz and 2MHz Clock signals to the appro-

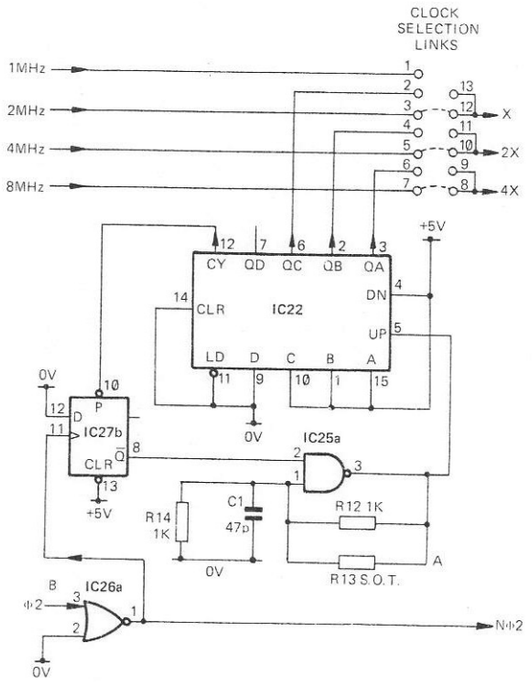


Figure 7. Clock Circuit

priate 4X, 2X and X outputs. The local oscillator circuit is not used in this case. To operate at 1 MHz the links must be removed and the required links soldered in place.

2.3.2 Local Oscillator Operation

To operate from the local oscillator the appropriate Clock Selection Links must be connected, refer to Table 2. The negative edge of the §2 signal from the CPU is inverted by NOR gate IC26a to clock D-type bistable IC27b, refer to Figure 7. The Q output of IC27b goes high since the D input is connected to 0V. The high on Q enables the local oscillator, NAND gate IC25a, R12, R13, R14 and C1. The oscillator output clocks binary counter IC22, to produce the 4MHz, 2MHz and 1MHz Clock signals, refer to timing diagram, Figure 8.

INPUT		CLOCK SELECTION LINKS	OUTPUT SIGNAL
ACORN BUS	LOCAL OSC.		
8MHz	—	7 to 8	4X
4MHz	—	5 to 10	2X
2MHz	—	3 to 12	X
4MHz	—	5 to 9	4X
2MHz	—	3 to 11	2X
1MHz	—	1 to 13	X
—	4MHz	6 to 9	4X
—	2MHz	4 to 11	2X
—	1MHz	2 to 13	X

Table 2. Clock Selection Links

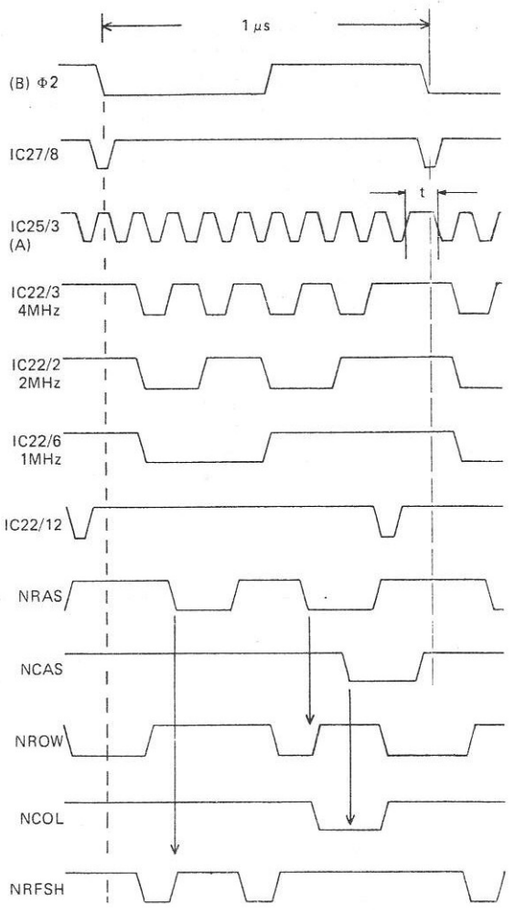


Figure 8. 32K DRAM Clock Timing (Local Oscillator/§2 Synchronization)

When the binary counter reaches a count of F (hex) the CY output goes low to the preset input of D-type bistable IC27b. IC27b Q output goes low to load 7 (hex) into the data inputs of IC22, and also to inhibit the local oscillator output from IC25a. The next §2 negative edge clocks IC27b to restart the local oscillator and count up IC22 from 7, thus synchronizating the local oscillator.

2.3.3 Local Oscillator Setting-Up Procedure

To set up the local oscillator the select on test resistor (R13) is used to adjust the frequency of the clock circuit. The value of R13 should be in the order of 1kOhm.

The following equipment is required:

Dual-beam oscilloscope
Variable +5V power supply
Frequency Generator

Connect the oscilloscope as follows (refer to Figure 7):

Channel A to right hand end of R13 or IC25/3(A).
Channel B to §2, IC26/3(B).

Set the oscilloscope to:

Amplitude	2V/cm
Timebase	100ns/cm
Trigger	Channel B

Connect the power supply to the board edge connector as follows:

+5V to Side A pin 1
0V to Side A pin 32

Set the power supply output to +5.0V.

Connect the frequency generator output to the board edge connector Side A pin 29 and 0V to Side A pin 32. Adjust the frequency generator output to 1.00MHz, amplitude +3.5V w.r.t. 0V.

Ensure that the length of the part "t" of the channel A trace in Figure 8 is 120ns +20ns at 50% amplitude.
-0ns

Adjust the power supply input to +4.5V and ensure that "t" is approximately 60ns.

Substitute different values of resistor R 13 until the above measurements are obtained.

2.4 REFRESH CIRCUIT

The Refresh Circuit consists of a dual 4 bit binary counter IC20 and an octal buffer IC19. The counter is configured to produce the 128 refresh addresses on the seven DRAM IC address lines CA0—CA6. The X clock signal (1MHz or 2MHz) from the Clock Selection Links clocks the counter on each negative edge. The octal buffer is enabled by the NRFSH signal low from the Memory Address Selection Circuit, so that a row address is loaded onto CA0—CA6 to be strobed into the DRAM ICs by the NRAS signal, refer to timing diagram, Figure 3. The DRAM IC refresh cycle is thus completed in 256µs (1MHz operation) or 128µs (2MHz operation).

2.5 DATA BUFFER

The Data Buffer is an octal buffer IC24. The buffer is enabled for data transmission by the NDEN signal low from the Memory Address Selection Circuit, refer to para 2.2.2. The direction of transmission of data is determined by the R/W signal on the Acorn Bus. The R/W signal is inverted by IC26b to select output from the 32K Dynamic RAM Board for a CPU Read operation, R/W high. R/W is low for Write to DRAM operation.

3. SOFTWARE PARAMETERS

3.1 MEMORY ADDRESSING

The 32K Dynamic RAM Board is provided with soldered links which give the Dynamic RAM the addresses 2000 to 7FFF (hex) and C000 to DFFF (hex), Acorn Memory Blocks 2 to 7, C arid D. If alternative addresses are required, refer to para 2.2.1.

3.2 MEMORY PAGING

The Link LK is supplied with a track connection on the 32K Dynamic RAM Board. When memory paging is required the track must be cut, the Valid Memory Address (NVMA) signal low can then be used to select the memory on the Board.

4. 32K DYNAMIC RAM BOARD CONNECTIONS

4.1 32K DYNAMIC RAM BOARD TO ACORN BUS

Pin	Mnemonic	Meaning	I/O
Side A			
1	+5V	+5V Supply	I
2	A15		
3	A14		
7	A8		
8	A7		
9	A6		
10	A5	Address Lines	I
11	A4		
12	A3		
13	A2		
14	A1		
15	A0		
16	D7		
17	D6		
18	D5		
19	D4		
20	D3	Data Lines	I/O
21	D2		
22	D1		
23	D0		
24	A13		
25	A12		
26	A11	Address Lines	I
27	A10		
28	A9		

Pin	Mnemonic	Meaning	I/O
Side A			
29	Φ2	Phase Two Clock	I
30	R/NW	Read/Write	I
32	0V	0V Supply	I

Pin	Mnemonic	Meaning	I/O
Side B			
14	8MHz	System Clocks	I
16	4MHz		
18	2MHz		
21	1MHz		
24	NVMA	Valid Memory Address	I
32	0V	0V Supply	I

5. PARTS LIST

5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
	PCB 200.100 Issue 4		1	
	PCB Terminals Vero 20-2137D (for R13)		2	
	20 pin IC Socket		4	
	16 pin IC Socket		19	
	14 pin IC Socket		4	

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
C1	Capacitor, Disc Ceramic	47pF	1	
C2	Capacitor, Electrolytic	22µF 16V	1	
C3...C14	Capacitor	47nF	12	
C15	Capacitor, Disc Ceramic	100pF	1	
PL1	Connector 64-way Plug (Right angle solder tails to DIN 41612)		1	
IC1...IC16	Integrated Circuit	4816-7 (for 1MHz)	16	
or	Integrated Circuit	4816-3 (for 2MHz)		
IC17...IC19	Integrated Circuit	74LS244	3	
IC20	Integrated Circuit	74LS393	1	
IC21	Integrated Circuit	74LS139	1	
IC22	Integrated Circuit	74LS193	1	
IC23	Integrated Circuit	74LS138	1	
IC24	Integrated Circuit	74LS245	1	
IC25	Integrated Circuit (Texas device only)	74LS132	1	
			1	
IC26	Integrated Circuit	74LS02	1	
IC27	Integrated Circuit	74LS74	1	
R1...R11	Resistor	33Ohm CR25	11	
R12	Resistor	lkOhm	1	
R13	Resistor	Select on test*	1	
R14	Resistor	100Ohm	1	
R15...R18	Resistor	3.3kOhm	4	
R19...R26	Resistor	68Ohm CR25	8	

*refer to para 2.3.3

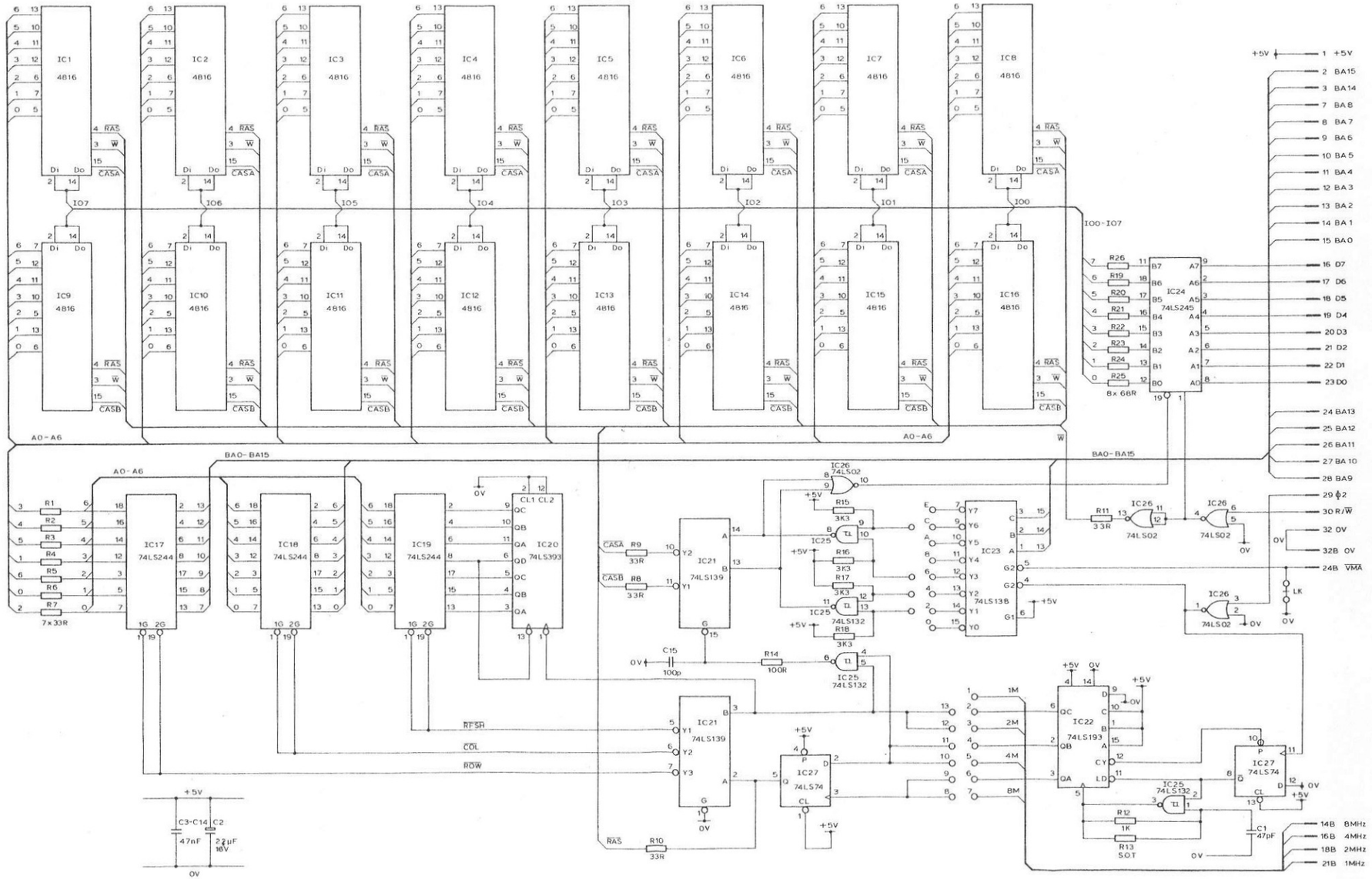


Figure 9. 32K Dynamic RAM Board Circuit Diagram